(19) World Intellectual Property Organization

International Bureau



(43) International Publication Date 6 October 2005 (06.10.2005)

PCT

(10) International Publication Number WO 2005/093955 A1

(51) International Patent Classification?: 7/089, H03D 13/00

H03L 7/087,

(21) International Application Number:

PCT/IB2005/050924

(22) International Filing Date: 16 March 2005 (16.03.2005)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data: 04101278.2

29 March 2004 (29.03.2004)

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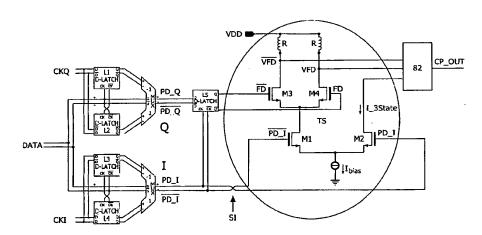
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE. AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ,

[Continued on next page]

(54) Title: FAST PHASE-FREQUENCY DETECTOR ARRANGEMENT



(57) Abstract: The present invention relates to a detector arrangement and a charge pump circuit for a recovery circuit recovering timing information for random data. The detector arrangement comprises first latch means for sampling a quadrature component of a reference signal based on an input signal, to generate a first binary signal, a second latch means for sampling an in-phase component of the reference signal based on the input signal, to generate a second binary signal, and a third latch means for sampling the first binary signal based on the second binary signal, to generate a frequency error signal. Thus, a simple and fast detection circuitry can be achieved based on a digital implementation. Furthermore, the charge pump circuit comprises a differential input circuit and control means for controlling a tail current of the differential input circuit in response to a frequency-locked state of frequency detector arrangement. This provides the advantage that behavior of the charge pump circuit can alleviate extra ripple generated by the detector arrangement.



CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

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